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MADAMBA, GLENFORD J	

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2451	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/822,896	MINAMI ET AL.	
	Examiner	Art Unit	
	Glenford Madamba	2451	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 February 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to remarks filed by Applicant's representative on January 16, 2009.

Response to Remarks and Arguments

2. Applicant's arguments and remarks filed January 16, 2009 have been fully considered but are deemed unpersuasive to overcome the rejection of the claims in view of the current grounds of rejection and the applied prior art reference(s). The Office maintains that the all the argued features of the claimed invention are taught and/or disclosed by the combination of Illikkal and Banerjee in accordance with the present claim recitation.

With regards to claims 1, 11 and 21, and claim 1 in particular, Applicant firstly argues that the Illikkal prior art reference does not teach or disclose particular features of the claim, which currently recites in part "wherein the control block (CB) cache is a multi-port device providing direct access to the CB cache via each port". In support of his argument, Applicant argues that "the mere disclosure of a NIC with a provided TCP/IP offload engine and an included TCB Cache, as in Illlikkal, simply fails to suggest applicant's claimed technique" and that "a NIC with a TCP/IP Offload Engine and a local TCB Cache, simply fails to suggest that the CB cache is a multi-port device, as claimed

by applicant". Applicant also argues with respect to claim 21 that such a disclosure of "a NIC with a TCP/IP Offload Engine and a local TCB Cache, simply fails to suggest applicant's claimed "multi-port SRAM control block (CB) cache in a transport offload engine(TOE), as claimed by applicant". The Office respectfully disagrees and submits that argued features are in fact sufficiently taught or suggested by Illikkal, in accordance with the claim recitation.

In response to applicant's above arguments, the Office remarks that Illikkal's express disclosure of a "NIC device comprising a TCP/IP Offload Engine (TOE) and a Transport Control Block (TCB) Cache" is not only significant in that it expressly discloses applicant's claimed "*Apparatus* for accessing and maintaining socket control information for high speed network connections *comprising a Control Block (CB) Cache in a Transport Offload Engine (TOE)*", it also discloses, as a consequence, the claimed "multi-port CB cache device" or "multi-port SRAM control block (CB) cache" component comprising the claimed 'apparatus'. In this regard, the Office asserts that Illikkal's teaching of a "*NIC device* comprising the claimed components of a *Control Block (CB) Cache* in a *Transport Offload Engine (TOE)*" expressly discloses applicant's claimed "apparatus…comprising a mechanism for storing socket control information in a control block (CB) in a transport offload engine (TOE)".

Illikkal's above disclosure also essentially discloses the argued feature of "wherein the CB cache is a multi-port device…" or a "multi-port SRAM control block (CB) cache in a transport offload engine (TOE)". In this regard, the Office asserts that the positive disclosure by Illikkal of a Control Block (CB) cache in a TCP/IP Offload Engine of a NIC device also accordingly / essentially discloses the presence of a 'multi-port device' or 'multi-port SRAM' that embodies the disclosed Control Block (CB) cache – by virtue of its inherency with respect to a TCP/IP Offload Network Interface Device, for example.

In this regard the Office notes with emphasis that the use of modular memory / embedded RAM in telecommunication circuitry and, in particular, digital integrated chips (ICs) for 'application' to registers, processors, buffers, and *caches*, is common technology and "well-known in the art". Disclosure of a Control Block (CB) cache as a component / part of a network interface device that stores in memory 'transfer control block' data also necessarily discloses the 'memory module' that embodies the cache component (i.e., SRAM module).

As such, the Office asserts that it is inherent for a NIC device 'performing the role of' or functioning as a "TCP/IP Offload Network Interface Device" and comprising a Control Block (CB) Cache, to have a memory module such as an SRAM component embodying the said cache component. In support of this assertion, the Office invites

Applicant to review disclosures to Sharp et al, US Patent Publication 2005/018241, cited but not referred to, and provided with this action as supplemental / evidentiary support for such an assertion. With reference to Fig. 1, for example, Sharp clearly and expressly discloses a exemplary 'TCP/IP Network Interface Device' comprising an ASIC chip, the integrated circuit chip further comprising a TCB Cache embodied by an SRAM component.

In this regard, the Office additionally asserts that it is also well-known in the art for an SRAM component embodying a 'cache', a register, a buffer, etc. to be a 'single-port' or 'multi-port' memory module. In support of this assertion, the Office invites Applicant to review non-patent literature to Silburt et al, "A 180-Mhz Modular Memory Family of DRAM and Multiport SRAM", published in 1993, also cited but not referred to, and provided with this action as supplemental / evidentiary support for such an assertion . The reference expressly discloses "a family of modular memories with a built-in self-test interface whose design is ideally suited to modular memories embedded within synchronous systems. The basic port design is self-contained and extensible to any number of ports sharing access to a common-core cell array. The same 'design' has been used to implement modular one-, two-, and four-port SRAMs", for example.

Moreover, Silburt also expressly teaches as a well-known feature / implementation of SRAM ports the mechanism for 'dedicated ports' (e.g., READ / WRITE dedicated ports) that have been incorporated in the design of a multi-port SRAM

(Silburt: Section IV Multiport Implementation) [pg. 226]. The argued features of "wherein a first port is dedicated to transmit logic within the TOE" and "wherein a second port is dedicated to receive logic within the TOE" is also therefore disclosed by Illikkal, and by features 'inherent to' Illikkal's disclosed "TCP/IP Offload NIC device" comprising a TCP/IP Offload Engine (TOE) and a TCB Cache. The Office thus maintains its rejection of claims 1, 4, 11 and 21 for at least these reasons.

With respect to claim 8, Applicant argues that neither Illikkal nor Banerjee teaches or discloses the recited feature of a "comparing the received network packet hash value with the hash values in a hash reference table". In support of his argument, Applicant remarks that Banerjee's express disclosure of "searching a hash table, in addition to storing and finding associated PCBs in a hash table", simply fails to suggest the recited feature of "comparing the received network packet hash value with the hash values in the hash reference table". The Office respectfully disagrees.

In response to the argument, the Office notes and remarks that with reference to Figures 4 & 5 of Banerjee, Banerjee expressly discloses a process flow chart with 'steps' which include identifying / creating a PCB for a received packet (steps 502-508) storing a PCB entry associated with a socket in a PCB Cache (step 414), searching a *PCB hash table* to locate a PCB and do connection processing / using the PCB to locate appropriate socket and do connection processing (steps 516-517), as well as the steps of 'identifying a lowest PCB entry stored in the PCB cache (step 526) and

removing the lowest priority PCB from the PCB cache and storing it in the regular PCB hash table (step 528).

Based on the above disclosures, it is clear that the disclosed steps of 'generating' (402) and 'storing a PCB in a hash table' (406), at the very least, teaches that a PCB entry is created for a packet, and then entered into a PCB 'Hash Table'. It is thus clear that the individual 'entries' of a *PCB Hash Table* are themselves necessarily 'hashed' or must have a field / parameter component comprising a 'hash value'. As such, it is thus obvious to one of ordinary skill that 'searching' a PCB Hash Table to identify or 'locate' a particular PCB (specific PCB 'hashed' entry or PCB with a 'hash value' parameter) associated with a 'connection' and in relation to the receipt of a packet, clearly implies that the PCB 'hash value' of a received packet is being 'matched' or compared to 'hashed' entries of a PCB Hash Table to identify / locate the particular PCB. The argued feature is thus expressly disclosed by at least Banerjee, and the Office maintains its rejection of the claim for at least this reason.

With respect to claim 22, Applicant argues that neither Illikkal nor Banerjee teaches or discloses the recited feature of a "mechanism for arbitrating access between TOE clients sharing a common port in a multi-device based on a priority". In support of his argument, Applicant remarks that merely disclosing that a priority may be assigned to each socket, where PCBs associated with high priority sockets are stored in the PCB cache, as in Banerjee, simply fails to teach or suggest the above said recited feature. The Office respectfully disagrees.

In response to the argument, the Office firstly remarks that it has been previously demonstrated above for claims 1, 11 and 21 that Illikal expressly discloses an apparatus comprising a multi-port Control Block (CB) cache and transport offload engine (TOE). Banerjee provides the added features and expressly discloses for example that (1) PCBs (associated with a received packet requesting access / connection) may be 'prioritized' [Abstract], (2) that a 'priority' may be assigned to each socket and thus to the PCB associated with the socket; and (3) that connection requests such as 'WEB requests' may be assigned a higher priority that other connection (thus a WEB server port number is assigned a high priority in order to deliver high performance). As such, the Office asserts that it is obvious to one of ordinary skill that the combination of these disclosures clearly teaches or suggests the "arbitration" logic / mechanism for deciding which among a plurality of client requesting access from a shared / common port should be granted the 'connection' or access to the shared port (i.e., by 'priority' of the PCBs associated with the packets transmitted by each of the respective clients). The argued feature of a "mechanism for arbitrating access between TOE clients sharing a common port in a multi-device based on a priority" is thus disclosed by the combination of Illikkal and Banerjee, and the Office maintains its rejection of the claim for at least the reasons above.

Having established that all of applicant's argued features are disclosed by the Illikkal and/or Banerjee prior art references, the Office maintains its rejection of the claims, and the present claims thus stand 'rejected'.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2, 4, 11, 12, 14 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Illikkal, U.S. Patent Publication US 2004/0019670 A1.

As per Claims 1, 11, and 21, Illikkal discloses a method of accessing and maintaining socket control information for high speed network connections, the method comprising the steps of:

storing socket control information (i.e., TCB Information 232) (e.g., TCB may include local remote socket numbers, etc.) [0015] in a control block (CB) cache (e.g.,

TCB Cache 280) [Fig. 2] in a transport offload engine (TOE) (e.g., Transport Offload Engine 20) [Fig. 2];

wherein CB entries in the CB cache are comprised of socket control information for sockets assigned to the TOE by a host computer (e.g., Server 200) [Fig. 2];

wherein the CB cache is a multi-port device providing direct access to the CB cache via each port [Fig. 2];

wherein a first port is dedicated to transmit logic within the TOE (e.g., 'SEND')[0038-0044]; and

wherein a second port is dedicated to receive logic within the TOE (e.g., 'RECEIVE') [0030-0036] [Fig. 7].

Claims 11 and 21 recite the same limitations as claim 1, are distinguished only by their statutory category, and thus rejected accordingly.

As per Claims 2 and 12, Illikkal discloses a method as recited in Claim 1, further comprising the step of:

dedicating a port to an optional memory(e.g., External Memory Unit 230) [Fig. 2];

wherein the optional memory stores the CB entries (e.g., TCB Information 232) that are directly accessible by the CB cache via the port (e.g., TCB Cache 280) [Fig.2]; and

wherein the optional memory also serves as main memory for the TOE [Fig. 2].

As per Claims 4 and 14, Illikkal discloses a method as recited in claim 1, further comprising the step of: dedicating a port for host transfers of the CB entries (e.g., Host Processor 210) [Fig. 2].

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3, 6, 8, 9, 10, 13, 16, 18, 19, 20, 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Illikkal in view of Banerjee et al (hereinafter Banerjee), U.S. Patent Publication US 2005/0114692 A1.

As per Claims 3 and 13, Illikkal in view of Banerjee discloses a method as recited in claim 2, wherein one entry in the CB cache is kept empty to facilitate reading a CB entry from the optional memory before writing the CB entry into the optional memory.

With regards to the claim, while Illikkal discloses substantial features of the invention, the additionally recited feature of the method wherein one entry in the CB cache is kept empty to facilitate reading a CB entry from the optional memory before writing a CB entry into the optional memory is taught by Banerjee in a related endeavor.

Banerjee discloses as his invention a method and system for improving the performance of a TCP connection [Abstract]. Specifically, Banerjee discloses the additionally recited feature of the method wherein one entry in the CB cache is kept empty to facilitate reading a CB entry from the optional memory before writing a CB entry into the optional memory (e.g. 'Unused Space' in PCB Cache 412 / 522) [Figs. 4 & 5].

It would thus be obvious to one of ordinary skill in the art at the time of the invention to modify and/or combine Illikkal's invention, with the above said feature, as disclosed by Banerjee, for the motivation of providing a system and method for improving computer network connection processing by prioritizing PCBs and storing frequently used or other high priority PCBs in a PCB cache whereby the high priority PCBs may be located quickly [0015].

Claim 13 recites the same limitations as claim 3, is distinguished only by statutory category, and thus rejected on the same basis.

As per Claims 6, 16 and 23, Illikkal in view of Banerjee discloses a method as recited in claim 1, further comprising the step of:

dedicating a port to low demand TOE clients [Fig. 2]; and

wherein the low demand TOE clients are granted access to the port based on a priority (Banerjee: e.g., PCBs may be 'prioritized' {High / Low Priority 'connection' with clients}) [Abstract] [Figs. 4 & 5].

With regards to the claim, while Illikkal discloses substantial features of the invention, the additionally recited feature of the method wherein the low demand TOE clients are granted access to the port based on a priority is taught by Banerjee in a related endeavor.

Banerjee discloses as his invention a method and system for improving the performance of a TCP connection [Abstract]. Specifically, Banerjee discloses the additionally recited feature of the method wherein the low demand TOE clients are granted access to the port based on a priority (e.g. PCBs may be 'prioritized' {High / Low Priority 'connection' with clients}) [Abstract] [Figs. 4 & 5].

It would thus be obvious to one of ordinary skill in the art at the time of the invention to modify and/or combine Illikkal's invention, with the above said feature, as disclosed by Banerjee, for the motivation of providing a system and method for improving computer network connection processing by prioritizing PCBs and storing frequently used or other high priority PCBs in a PCB cache whereby the high priority PCBs may be located quickly [0015].

Claims 16 and 23 recite the same limitations as claim 6, are distinguished only by statutory category, and thus rejected on the same basis.

As per Claims 8 and 18, Illikkal in view of Banerjee discloses a method as recited in claim 1, further comprising the steps of:

providing a hash reference table (Banerjee: e.g., 'store PCB in Hash Table' 406) [Fig. 4];

wherein the hash reference table is comprised of hash values corresponding to each CB entry in the CB cache (Banerjee: e.g., PCB Hash Table with 'pointer' 604 associated with a particular PCB in a linked list of the table) [0008] [0013] [Fig. 6];

creating a hash value for a received network packet (Banerjee: e.g., 'receive a packet' 502) [Fig. 5] (e.g., PCB 600) [0007-0008];

comparing the received network packet hash value with hash values in the hash reference table [Banerjee: 0020-0021]; and

searching for a corresponding CB entry in the CB cache via a port if the network packet hash value matches the hash value in the hash reference table [Banerjee: 0020-0021].

With regards to the claim, while Illikkal discloses substantial features of the invention, the additionally recited features of the method further comprising the steps of providing a hash reference table; wherein the hash reference table is comprised of hash values corresponding to each CB entry in the CB cache; creating a hash value for a

received network packet; comparing the received network packet hash value with hash values in the hash reference table; and searching for a corresponding CB entry in the CB cache via a port if the network packet hash value matches a hash value in the hash reference table is taught by Banerjee in a related endeavor.

Banerjee discloses as his invention a method and system for improving the performance of a TCP connection [Abstract]. Specifically, Banerjee discloses the additionally recited features of the method further comprising the steps of providing a hash reference table (Banerjee: e.g., 'store PCB in Hash Table' 406) [Fig. 4]; wherein the hash reference table is comprised of hash values corresponding to each CB entry in the CB cache (Banerjee: e.g., PCB Hash Table with 'pointer' 604 associated with a particular PCB in a linked list of the table) [0008] [0013] [Fig. 6]; creating a hash value for a received network packet (Banerjee: e.g., 'receive a packet' 502) [Fig. 5] (e.g., PCB 600) [0007-0008]; comparing the received network packet hash value with hash values in the hash reference table [Banerjee: 0020-0021]; and searching for a corresponding CB entry in the CB cache via a port if the network packet hash value matches a hash value in the hash reference table [Banerjee: 0020-0021].

It would thus be obvious to one of ordinary skill in the art at the time of the invention to modify and/or combine Illikkal's invention, with the above said feature, as disclosed by Banerjee, for the motivation of providing a system and method for improving computer network connection processing by prioritizing PCBs and storing frequently used or other high priority PCBs in a PCB cache whereby the high priority PCBs may be located quickly [0015].

Claim 18 recites the same limitations as claim 8, is distinguished only by statutory category, and thus rejected on the same basis.

As per Claims 9, 10, 19 and 20, Illikkal in view of Banerjee discloses a method as recited in Claim 1, further comprising the steps of:

providing a CB identifier reference table (Banerjee: e.g., PCB Hash Table) [0013];

wherein the CB identifier reference table is comprised of a unique CB identifier corresponding to each CB entry in the CB cache and an associated CB cache index (Banerjee: e.g., PCB Hash Table with 'pointer' 604 associated with a particular PCB in a linked list of the table) [0008] [0013] [Fig. 6];

creating a CB identifier by parsing out the CB identifier from a CB access address [Banerjee: 0007-0008] [Fig. 6];

comparing the CB identifier with CB identifier values in the CB identifier reference table [Banerjee: 0020-0021];

accessing the CB cache via a port using the CB cache index of a matching CB identifier value in the CB identifier reference table (Banerjee: e.g., port 80) [0020-0021]; and

wherein if the CB identifier does not match the CB identifier value in the CB identifier reference table, then the corresponding socket has either not been assigned to the TOE or the CB entry must be brought into the CB cache from an optional memory [Banerjee: 0020-0021].

With regards to the claims, while Illikkal discloses substantial features of the invention, the additionally recited features of the method further comprising the steps of providing a CB identifier reference table; wherein the CB identifier reference table is comprised of a unique CB identifier corresponding to each CB entry in the CB cache and an associated CB cache index; creating a CB identifier by parsing out a CB identifier from a CB access address; comparing the CB identifier with CB identifier values in the CB identifier reference table; accessing the CB cache via a port using the CB cache index of a matching CB identifier value in the CB identifier reference table; and wherein if the CB identifier does not match a CB identifier value in the CB identifier reference table, then the corresponding socket has either not been assigned to the TOE or the CB entry must be brought into the cache from an optional memory is taught by Banerjee in a related endeavor.

Banerjee discloses as his invention a method and system for improving the performance of a TCP connection [Abstract]. Specifically, Banerjee discloses the additionally recited features of the method further comprising the steps of providing a CB identifier reference table (Banerjee: e.g., PCB Hash Table) [0013]; wherein the CB identifier reference table is comprised of a unique CB identifier corresponding to each CB entry in the CB cache and an associated CB cache index (Banerjee: e.g., PCB Hash Table with 'pointer' 604 associated with a particular PCB in a linked list of the table) [0008] [0013] [Fig. 6]; creating a CB identifier by parsing out a CB identifier from a CB access address [Banerjee: 0007-0008] [Fig. 6]; comparing the CB identifier with CB

identifier values in the CB identifier reference table [Banerjee: 0020-0021]; accessing the CB cache via a port using the CB cache index of a matching CB identifier value in the CB identifier reference table (Banerjee: e.g., port 80) [0020-0021]; and wherein if the CB identifier does not match a CB identifier value in the CB identifier reference table, then the corresponding socket has either not been assigned to the TOE or the CB entry must be brought into the cache from an optional memory [Banerjee: 0020-0021].

It would thus be obvious to one of ordinary skill in the art at the time of the invention to modify and/or combine Illikkal's invention, with the above said feature, as disclosed by Banerjee, for the motivation of providing a system and method for improving computer network connection processing by prioritizing PCBs and storing frequently used or other high priority PCBs in a PCB cache whereby the high priority PCBs may be located quickly [0015].

Claim 19 recites the same limitations as claim 9, is distinguished only by statutory category, and thus rejected on the same basis.

Claims 10 and 20 recite the same limitations as claims 9 and 19, except for the additional recited feature of providing means for retrieving a corresponding CB entry from the optional memory and placing the retrieved CB entry in the CB cache, if the CB cache index of the matching CB identifier value indicates that the CB entry is not in the CB cache, which is also expressly disclosed by Banerjee [Figs 4-7].

As per claim 22, Illikkal in view of Banerjee discloses an apparatus as recited in claim 21, further comprising: a mechanism for arbitrating access between TOE clients sharing a common port in a multi-port device based on a priority; and wherein time critical TOE clients are assigned a higher priority.

With regards to the claim, while Illikkal discloses substantial features of the invention, the additionally recited feature of the apparatus further comprising a mechanism for arbitrating access between TOE clients sharing a common port in the multi-port device based on a priority, wherein time critical TOE clients are assigned a higher priority is taught by Banerjee in a related endeavor.

Banerjee discloses as his invention a method and system for improving the performance of a TCP connection [Abstract]. Specifically, Banerjee discloses the additionally recited feature of of the apparatus further comprising a mechanism for arbitrating access between TOE clients sharing a common port (Banerjee: e.g, port 80) [0020] in the multi-port device based on a priority, wherein time critical TOE clients are assigned a higher priority (Banerjee: e.g., certain 'requests', such as WEB requests, may be assigned a higher priority than other connections) [Abstract] [0019-0021].

It would thus be obvious to one of ordinary skill in the art at the time of the invention to modify and/or combine Illikkal's invention, with the above said feature, as disclosed by Banerjee, for the motivation of providing a system and method for improving computer network connection processing by prioritizing PCBs and storing

frequently used or other high priority PCBs in a PCB cache whereby the high priority PCBs may be located quickly [0015].

5. Claims 5, 7, 15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Illikkal in view of Boucher et al (hereinafter Boucher), U.S. Patent Publication US 2002/0156927 A1.

As per Claims 5 and 15, Illikkal in view of Boucher discloses a method as recited in claim 1, wherein the CB entries are read from the CB cache in a word order that is dependent upon a port's purpose.

With regards to the claim, while Illikkal discloses substantial features of the invention, the additionally recited feature of the method wherein CB entries are read from the CB cache in a word order that is dependent upon a port's purpose is taught by Boucher in a related endeavor.

Boucher discloses as his invention a method and system for improving the performance of a TCP connection [Abstract]. Specifically, Boucher discloses the additionally recited feature of the method wherein CB entries are read from the CB cache in a word order that is dependent upon a port's purpose (e.g., creating a 'word' or 'words' which identify a message packet….) [0043-0044] [0046] [Fig. 4c].

It would thus be obvious to one of ordinary skill in the art at the time of the invention to modify and/or combine Illikkal's invention, with the above said feature, as disclosed by Boucher, for the motivation of providing a system and method for processing network communication that greatly increases the speed of that processing and the efficiency of moving the data being communicated [0012].

Claim 15 recites the same limitations as claim 5, is distinguished only by statutory category, and thus rejected on the same basis.

As per Claims 7 and 17, Illikkal in view of Boucher discloses a method as recited in Claim 1, further comprising the step of: providing field locking means for locking a specific field within a CB entry that is being accessed by a port; wherein the locking means prevents other ports from accessing a locked field.

With regards to the claim, while Illikkal discloses substantial features of the invention, the additionally recited feature of the method further comprising the step of providing field locking means for locking a specific field within a CB entry that is being accessed by a port, wherein the locking means prevents other ports from accessing a locked field is taught by Boucher in a related endeavor.

Boucher discloses as his invention a method and system for improving the performance of a TCP connection [Abstract]. Specifically, Boucher discloses the

additionally recited feature of the method further comprising the step of providing field locking means for locking a specific field within a CB entry that is being accessed by a port, wherein the locking means prevents other ports from accessing a locked field (e.g., 'setting locks') [0092] (e.g, "LOCK STATUS") [0609].

It would thus be obvious to one of ordinary skill in the art at the time of the invention to modify and/or combine Illikkal's invention, with the above said feature, as disclosed by Boucher, for the motivation of providing a system and method for processing network communication that greatly increases the speed of that processing and the efficiency of moving the data being communicated [0012].

Claim 17 recites the same limitations as claim 7, is distinguished only by statutory category, and thus rejected on the same basis.

Conclusion

1. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenford Madamba whose telephone number is 571-272-7989. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Follansbee can be reached on 571-272-3964. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/John Follansbee/
Supervisory Patent Examiner, Art Unit 2451

Glenford Madamba
Examiner
Art Unit 2451